Ex parte Ryan

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 14

95-4951

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PAT & TM OFFICE
BOARD OF PATENT APPEALS
AND INTERFERENCES

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHARLES P. RYAN

Appeal No. 95-4951
Application 07/841,687[1]

ON BRIEF

Before THOMAS, KRASS and JERRY SMITH, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellant has appealed to the Board from the examiner's

final rejection of claims 7, 9 to 13, and 15 to 35.

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[1] Application for patent filed February 26, 1992. This application is a continuation-in-part of Application 07/364,943 filed June 12, 1989, issued on March 3, 1992 as U.S. Patent No. 5,093,777.

1

Claims 1 to 6, 8, and 14 were cancelled by appellant's amendment dated March 10, 1994.

Representative claim 29 is reproduced below:

29. The method for predicting operand addressees of operand requests in a data processing system in which a cache thereof is repeatedly interrogated to determine whether an operand address corresponding to a requested operand is stored therein, said cache storing operands and their corresponding operand addresses; wherein said data processing system includes a main memory; said method being carried out by said data processing system in operating said cache, characterized by the computer-implemented steps of:

(A) upon the generation of and interrogation of said cache by a request operand address,

(B) determining whether a plurality of earlier-generated request operand addresses correspond to one of a plurality of predetermined operand address patterns, and

(C) (1) if no one of said patterns is determined to correspond to said plurality of request operand addresses in step (B), returning to step (A), but

(2)   (i) if one of said patterns is determined to correspond to said plurality of request operand addresses, generating an operand address of a predicted operand request using said one pattern,

(ii) obtaining the operand from the main memory location represented by said predicted operand address and writing said operand into said cache, and

(iii) returning to step (A),

wherein said method of steps A-C is performed only during intervals which commence immediately after a process change and terminate upon the first occurrence of a succeeding predetermined event, which predetermined event occurs after the maximum rate of increase in the operative hit rate of said cache is reached following said process change.

The following references are relied on by the examiner:

"New Context Bit", IBM Technical Disclosure Bulletin, Volume 30, Number 2, July 1987, page 510. (the Bulletin).

Palmer   5,305,389   April 19, 1994
                                                (filed August 30, 1991)

Claims 7, 9 to 13, and 15 to 35 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to teach how to make and/or use the invention.

Claims 7, 9 to 13, and 15 to 35 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

Claims 7, 9 to 13, and 15 to 35 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon the Bulletin in view of Palmer.

Appeal No. 95-4951
Application 07/841,687

Rather than repeat the positions of the appellant and the

examiner, reference is made to the Brief and the Answer for the

respective details thereof.[2]

OPINION

We have carefully considered the entire record before us,

and we will reverse all of the rejections of claims 7, 9 to 13,

and 15 to 35.

35 U.S.C. § 112, First Paragraph Rejection

We turn first to the rejection of claims 7, 9 to 13, and 15

to 35 under 35 U.S.C. § 112, first paragraph, based on the

examiner's position that the disclosure does not adequately teach

how to make and use without undue experimentation the present

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[2] We note that the after final request for reconsideration
dated August 1, 1994, was entered and considered by the examiner
(see the advisory action dated August 10, 1994).
    We also note that the Reply Brief dated May 26, 1995 was
neither considered nor entered by the examiner (see the letter
from the examiner dated September 7, 1995).

4

invention set forth in these claims. The rejection is therefore based upon the enablement clause of this statutory provision.

To comply with the enablement clause of the first paragraph of 35 U.S.C. § 112, the disclosure must adequately describe the claimed invention so that the artisan could practice it without undue experimentation. In re Scarbrough, 500 F.2d 560, 566, 182 USPQ 298, 302 (CCPA 1974); In re Brandstadter, 484 F.2d 1395, 1407, 179 USPQ 286, 294-95 (CCPA 1973); In re Gay, 309 F.2d 769, 772, 135 USPQ 311, 315 (CCPA 1962). If the examiner had a reasonable basis for questioning the sufficiency of the disclosure, the burden shifted to the appellant to come forward with evidence to rebut this challenge. In re Doyle, 482 F.2d 1385, 1392, 179 USPQ 227, 232-33 (CCPA 1973), cert. denied, 416 U.S. 935 (1974); In re Brown, 477 F.2d 946, 950, 177 USPQ 691, 694 (CCPA 1973); and In re Ghiron, 442 F.2d 985, 992, 169 USPQ 723, 728 (CCPA 1971). However, the burden was initially upon the examiner to establish a reasonable basis for questioning the adequacy of the disclosure. In re Angstadt, 537 F.2d 498, 504,

190 USPQ 214, 219 (CCPA 1976); and In re Armbruster, 512 F.2d 676, 678, 185 USPQ 152, 154 (CCPA 1975).

We will not sustain this rejection. The examiner's reasoning for this rejection is set forth in the Answer at pages 3 to 5. We disagree with the examiner's positions that the disclosure is nonenabling as to how a "first predetermined number" and count information are determined, as to the details of the structure implementing the prefetch algorithm, as to how the "hit ratio threshold" is determined, and as to what constitutes a "process change."

Specifically, we find that appellant's figure 6 and the accompanying text at pages 16 to 17 of the specification (describing the operation of timer 51 and counter 52) adequately describe how a "first predetermined number" is determined such that the artisan could practice the invention without undue experimentation. The understanding of how a counter and timer would operate to enable and disable the prefetch algorithm is well within the scope of the ordinary artisan's knowledge.

We find that appellant's figures 5, 6, and 7 and the accompanying text in the specification adequately describe the cache prefetch algorithm. It would have been clear to the artisan that "when" to implement the prefetch algorithm would depend on the occurrence of a new process at time T1 as shown in figure 5. The cache miss prediction logic 50 of figures 6 and 7 shows how the prefetch algorithm is performed, and provides the structure for implementing the algorithm. Figures 3 and 4 even provide an expanded and detailed explanation as to how the prediction logic 50 works. In view of these details given in the appellant's disclosure, we cannot say that the artisan would have had to unduly experiment in order to make and/or use the claimed invention.

We find that the artisan would have been able to understand how the "hit ratio threshold" is determined and used without undue experimentation. Appellant's figure 7 and the accompanying text at pages 17 to 19, in conjunction with figure 5, adequately show how the hit ratio threshold is determined. The disclosure provides an explanation of the operation of logic block 55

7

including division circuit 57, hit ratio threshold storage block

56, and comparator 58. The enabling and disabling of cache miss

prediction logic 50 is determined based on "snapshots" of curve

42 (see figure 5).

We find that the artisan would have understood what

constitutes a "process change" in light of the typical data

processing system environment as shown in appellant's figure 1

and as discussed at pages 1 to 2 and 6 to 7 of the specification.

The ordinary artisan would have recognized that a "process

change" involves the implementation of a new process such as a

program by processor 14, requiring access to new operands from

main memory unit 13 and cache memory unit 12. We agree with the

appellant (Brief, page 14) that page 3, lines 8 to 15 of the

specification provide adequate details as to how the new process

effects a process change. We also agree with appellant's

position that the meaning of "process," and therefore what

constitutes a "process change," is well known among those of

ordinary skill in the data processing art. Therefore, we find

that implementing a "process change" would not have required undue experimentation by the artisan.

In summary, we are not convinced that the examiner had a reasonable basis for questioning the adequacy of the disclosure or that undue experimentation would have necessarily resulted for the artisan to make and use the claimed invention.

35 U.S.C. § 112, Second Paragraph Rejection

Turning next to the rejection of claims 7, 9 to 13, and 15 to 35 under 35 U.S.C. § 112, second paragraph, it is to be noted that to comply with the requirements of the cited paragraph, a claim must set out and circumscribe a particular area with a reasonable degree of precision and particularity when read in light of the disclosure and the teachings of the prior art as it would be by the artisan. See In re Johnson, 558 F.2d 1008, 1015, 194 USPQ 187, 194 (CCPA 1977) and In re Moore, 439 F.2d 1232, 1235, 169 USPQ 236, 238 (CCPA 1971).

We have reviewed the examiner's reasons in support of the rejection but are not convinced that the cited claims fail to

comply with the second paragraph of 35 U.S.C. § 112. We are in

basic agreement with the appellant's position on this issue as

expressed at pages 14 to 16 of the Brief. We consider the

"wherein . . ." clauses at the end of independent claims 7, 13,

19, 25, 28, and 29 to particularly point out and distinctly claim

the subject matter of the invention.[3] We also find that the

meaning of "process change," although broad, is not so indefinite

to an artisan as to refer to a cache related change. As

discussed earlier with respect to the § 112, first paragraph,

rejection the meaning of "process change" is not indefinite. We

do not see where this language of the claims on appeal would have

generated any ambiguity or confusion to the artisan.

Accordingly, the rejection of claims 7, 9 to 13, and 15 to

35 under 35 U.S.C. § 112, second paragraph, must be reversed.

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[3] We note that the examiner failed to respond to the
appellant's arguments with respect to the "wherein . . ." clause
in his Answer. See the "Response to Argument Re-Section 112,
Second Paragraph Rejection" section of the Answer, pages 9 to 10.

35 U.S.C. § 103 Rejection Over the Bulletin in view of Palmer

The examiner rejected claims 7, 9 to 13, and 15 to 35 under 35 U.S.C. § 103 over the Bulletin in view of Palmer (see Answer, pages 5 to 6; final rejection, pages 5 to 6). The examiner relied on the Bulletin to teach a cache miss prediction mechanism which is enabled only during a period following a process change, and on Palmer to teach the use of operands as opposed to instructions. The issue is whether or not the Bulletin teaches or suggests enabling a prediction mechanism following a process change, and then disabling a prediction mechanism upon the occurrence of a "predetermined event" (either the passage of time or the attainment of the hit ratio threshold).

We agree with the appellant, and we conclude that the Bulletin does not fairly teach or suggest the feature of all of the independent claims of disabling a prediction mechanism upon the occurrence of a predetermined event. We find that the Bulletin's mention of disabling the prefetch mechanism when a prefetch is not used within a "reasonable period of time" does not meet the claimed limitation of disabling upon the occurrence

11

of a predetermined event which "occurs after the maximum rate of

increase in the operative hit rate of said cache memory" as set

forth in each independent claim on appeal.

The examiner begs the question as to when the prediction

mechanism is disabled at the middle of page 11 of his Answer by

recognizing that appellant argued this point in the Brief.

Although we agree with the examiner that the Bulletin's

prediction mechanism is enabled after a process change, we will

not speculate as to the meaning of a "reasonable period of time"

as disclosed by the Bulletin and we cannot agree with the

examiner that the Bulletin teaches the same type of disabling

feature as the claimed invention. We find it to be too large of

a leap to say that a "reasonable period of time" (the Bulletin)

was meant to describe "after the maximum rate of increase in the

operative hit rate of said cache memory is reached" (appellant's

claims). The Bulletin does not contemplate and does not disclose

determining a cache hit rate as shown in appellant's figure 5.

We therefore conclude that the Bulletin does not fairly

teach or suggest the disabling feature of independent claims 7,

13, 19, 25, 28, and 29. We further conclude that the limitations
of the dependent claims are not "all obvious variations of the
well known techniques applied in the address prefetching or
prediction art" as asserted by the examiner (Answer, pages 11 to
12) since the use of a hit ratio and a predetermined period of
time in evaluating a predetermined event are more detailed
variations of calculating a "predetermined event" (which is not
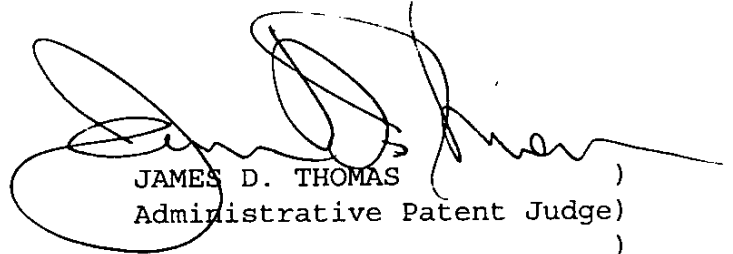taught or suggested by the Bulletin).

DECISION

In view of the foregoing, the decision of the examiner
rejecting claims 7, 9 to 13, and 15 to 35 under 35 U.S.C. § 112,
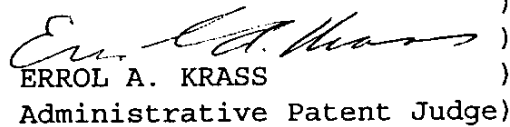first paragraph, is reversed.

The decision of the examiner rejecting claims 7, 9 to 13,
and 15 to 35 under 35 U.S.C. § 112, second paragraph, is also
reversed.

Lastly, the decision of the examiner rejecting claims 7, 9

to 13, and 15 to 35 under 35 U.S.C. § 103 is reversed.

<u>REVERSED</u>

JAMES D. THOMAS   )
Administrative Patent Judge)
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ERROL A. KRASS   )   BOARD OF PATENT
Administrative Patent Judge)   APPEALS AND
)   INTERFERENCES
)
)
JERRY SMITH   )
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14

Appeal No. 95-4951
Application 07/841,687

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